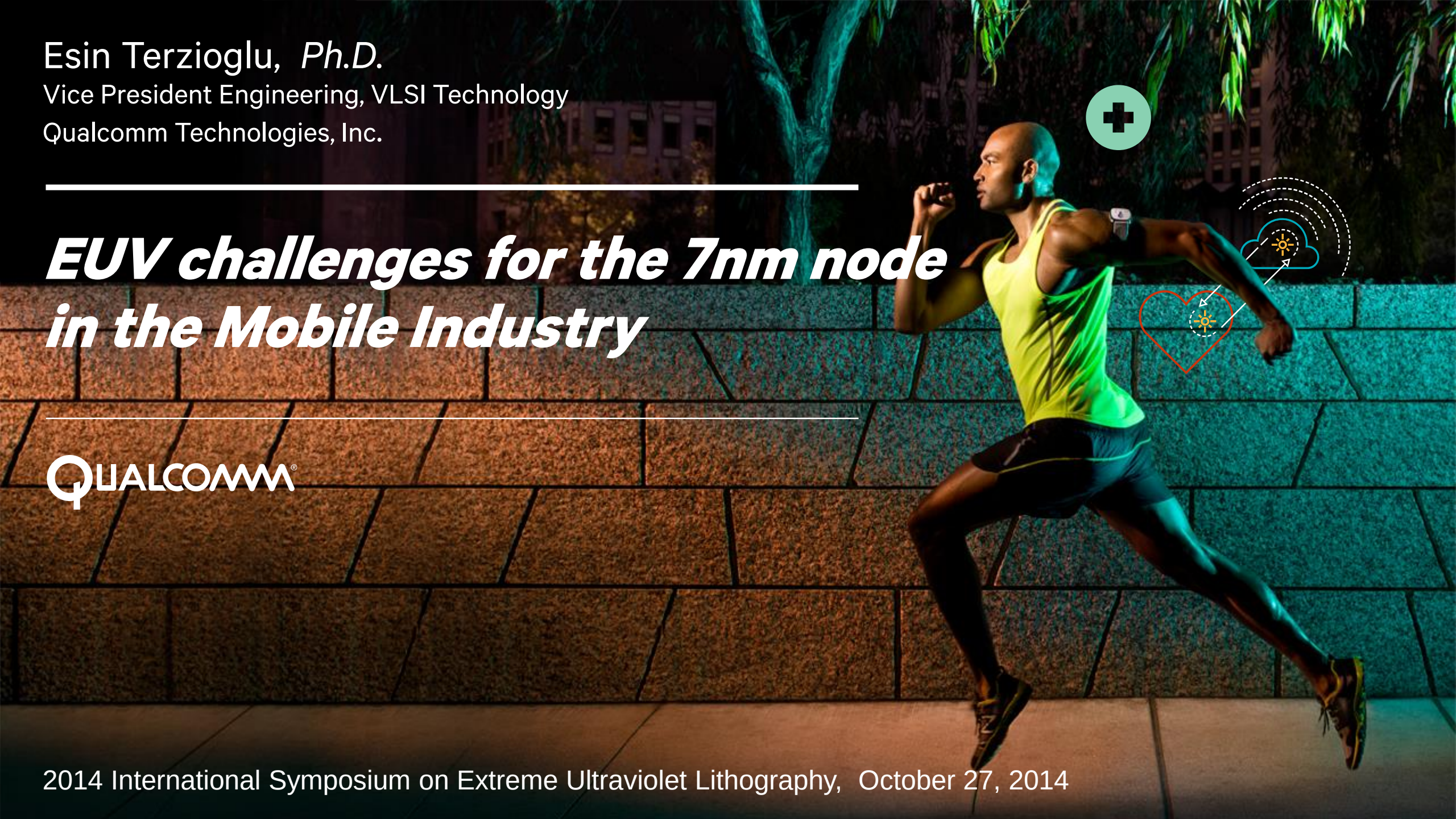
Esin Terzioglu, *Ph.D.*
Vice President Engineering, VLSI Technology
Qualcomm Technologies, Inc.

EUV challenges for the 7nm node in the Mobile Industry



QUALCOMM®

2014 International Symposium on Extreme Ultraviolet Lithography, October 27, 2014

Agenda

Mobile Revolution !

…and silicon technology requirements

Mobile Silicon Technology Roadmap

CMOS Scaling Cost Challenges

EUV and N7

Summary

Mobile Revolution !

Continued smartphone momentum

World's most pervasive technology platform

~8B

Cumulative smartphone unit shipments forecast between 2014-2018

Source: Gartner, Sept '13

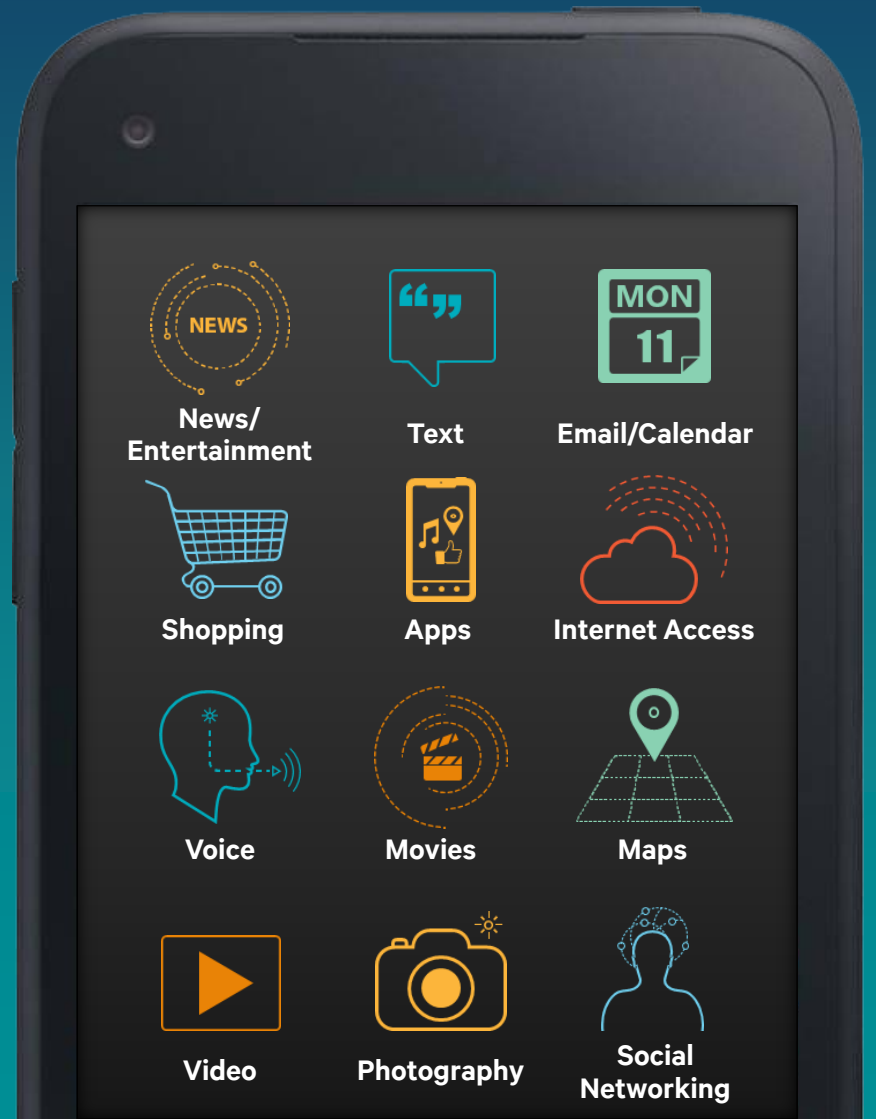
Smartphone: Our most personal + powerful device

~106

Avg. number of daily app launches by US Android users

~75%

18-24 year olds reach for it immediately after waking up



~94%

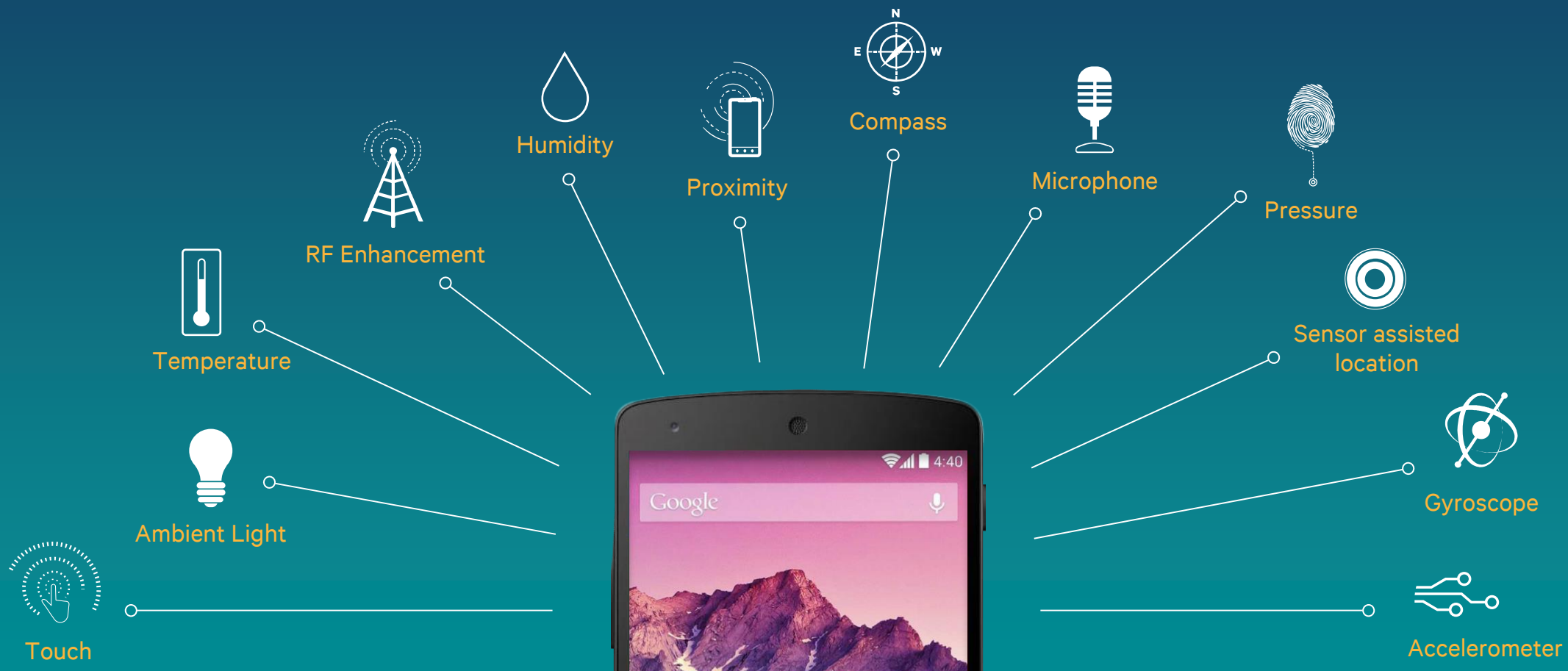
Use their device to look for local information

~79%

Watch video on their device

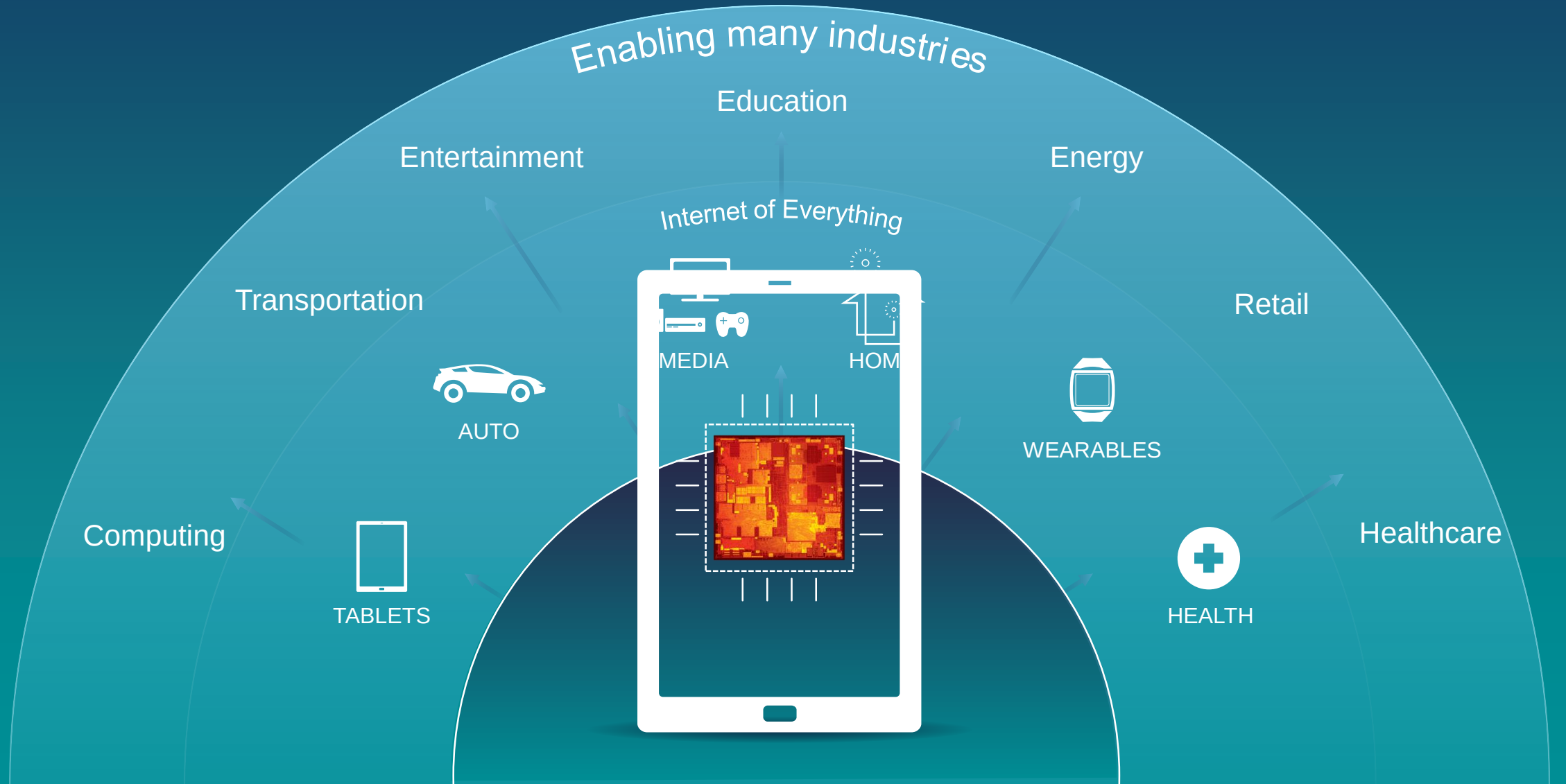
Sources: comScore custom research avg. over Q3'13, IDC Mar '13, Google May '13

Evolution of integrated sensors

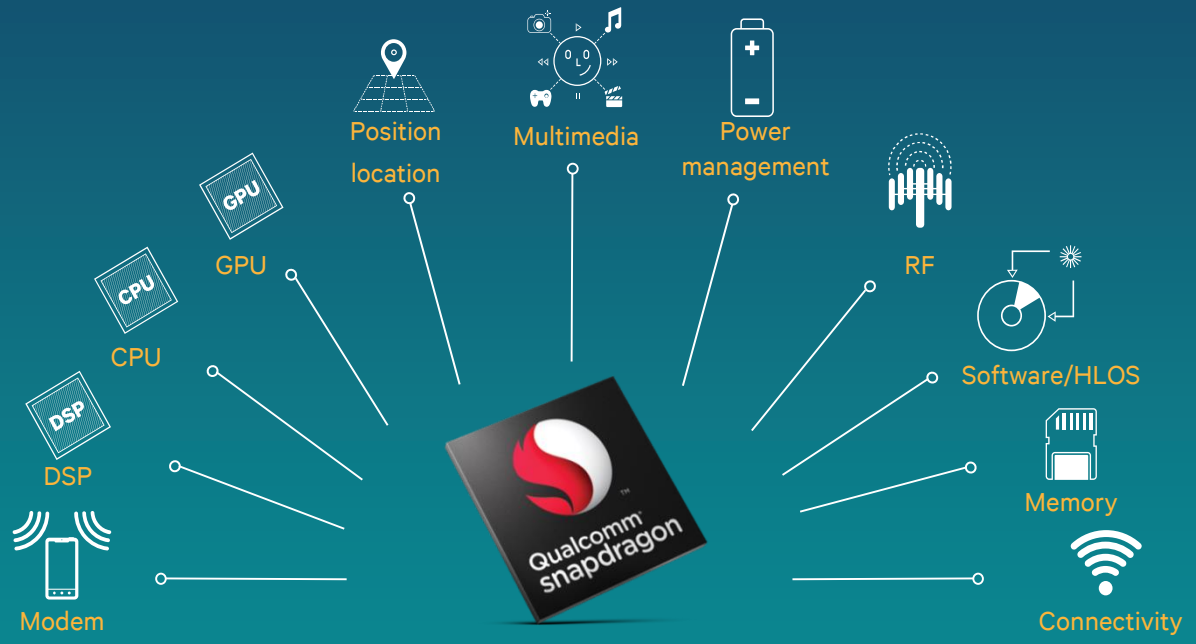


Environment **Navigation** **Context** **Health and fitness**

Expanding the mobile ecosystem beyond smartphones



Moving Forward: Thinner, Lighter, Sleeker.



Highly Integrated SoCs

Type 2: Perf + Multi-media + Connectivity

Type 1: Signal Processing + Connectivity

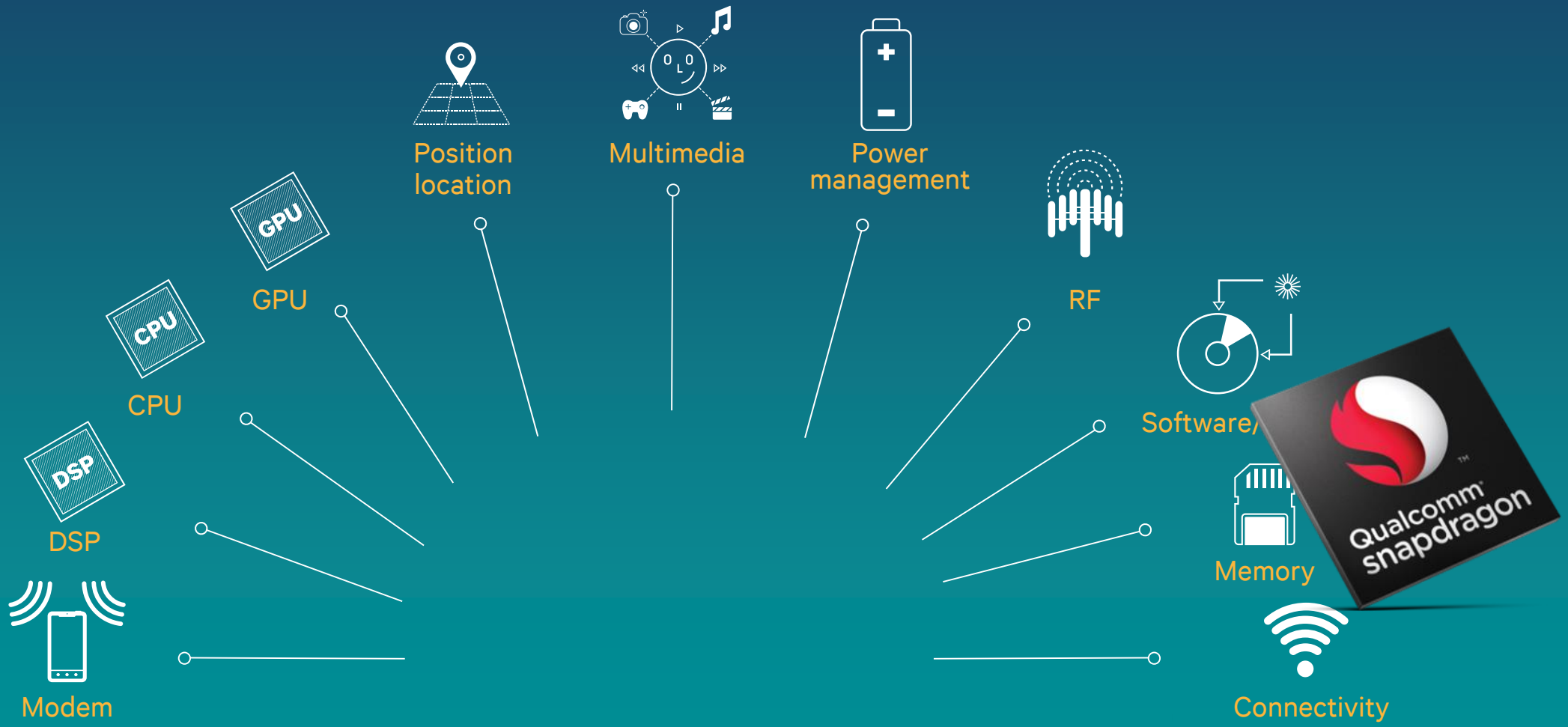
Packaging Innovation

e.g. PoP packages

Thermal Management

Friendly to body 24x7

Integrated system solutions for automotive




EVOLVING
TRANSPORTATION
~60% NEW CARS
shipped in 2017 will be connected through mobile technology
Source: ABI, 2013

TRANSFORMING HEALTH

45% REDUCTION

in mortality rate for chronic disease patients using telehealth

Source: U.K. Department of Health, Dec. '11

Connected Smarthome

>2X Connected Devices

in the household from 2013 to 2020

ENABLING **AWARENESS**

Capturing data about you and your environment

Source: Machina Research Apr ‘13

The future: Always **ON**. Always **SENSING**. Always **Connected**.

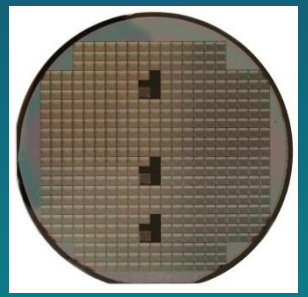
Environment **Navigation** **Context** **Health and fitness**

Always on: 1 Day => 1 Week => 1 Month Power Challenge

Low Power Architecture

Low Power Displays (e.g. Mirasol)

Aggressive Power Management



Low Power Process

2020 VISION

>25 BILLION

connected devices by2020

Source: Machina Research, '13

2020 VISION

- Always on
- Always connected
- Very low power
- Sensors everywhere
- Very hi degree of *cost-effective* integration

Technology Expectations

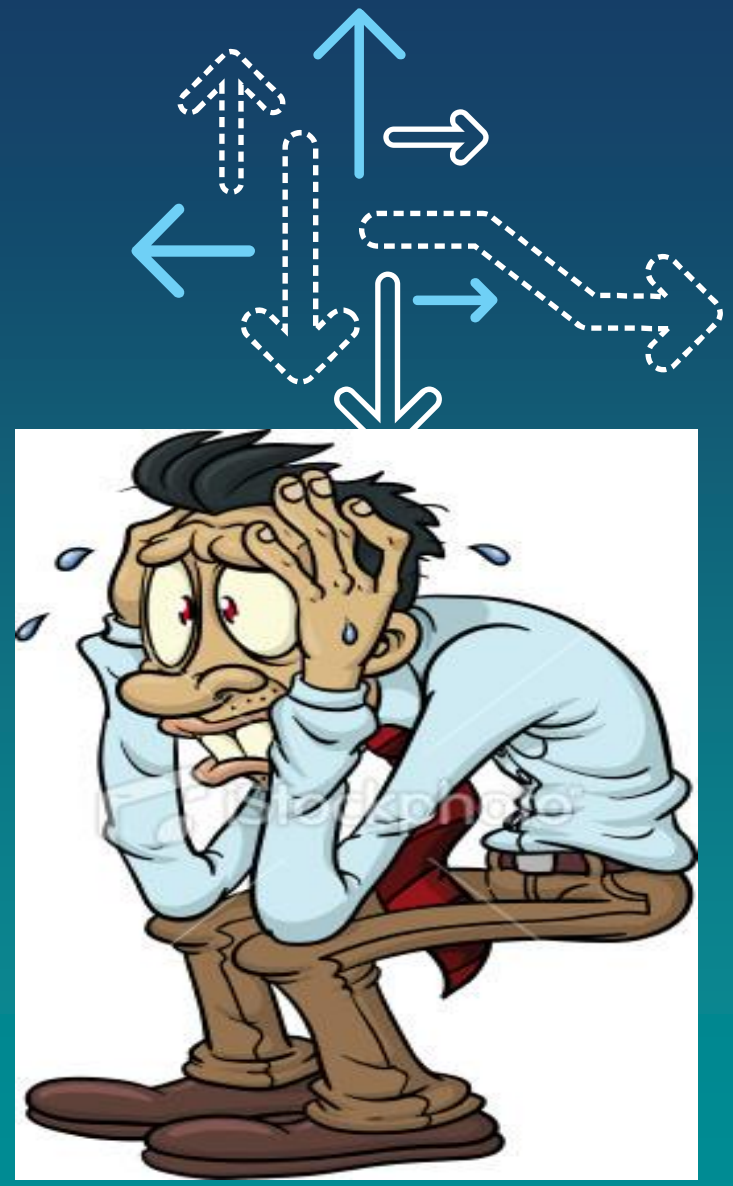
- Continuation of Moore's Law
  - -higher integration
  - -lower power
  - -lower cost
- Increasing "More than Moore"

THE INTERNET OF EVERYTHING

Source: Machina Research, '13

Continuing CMOS Scaling

Die Cost Worries



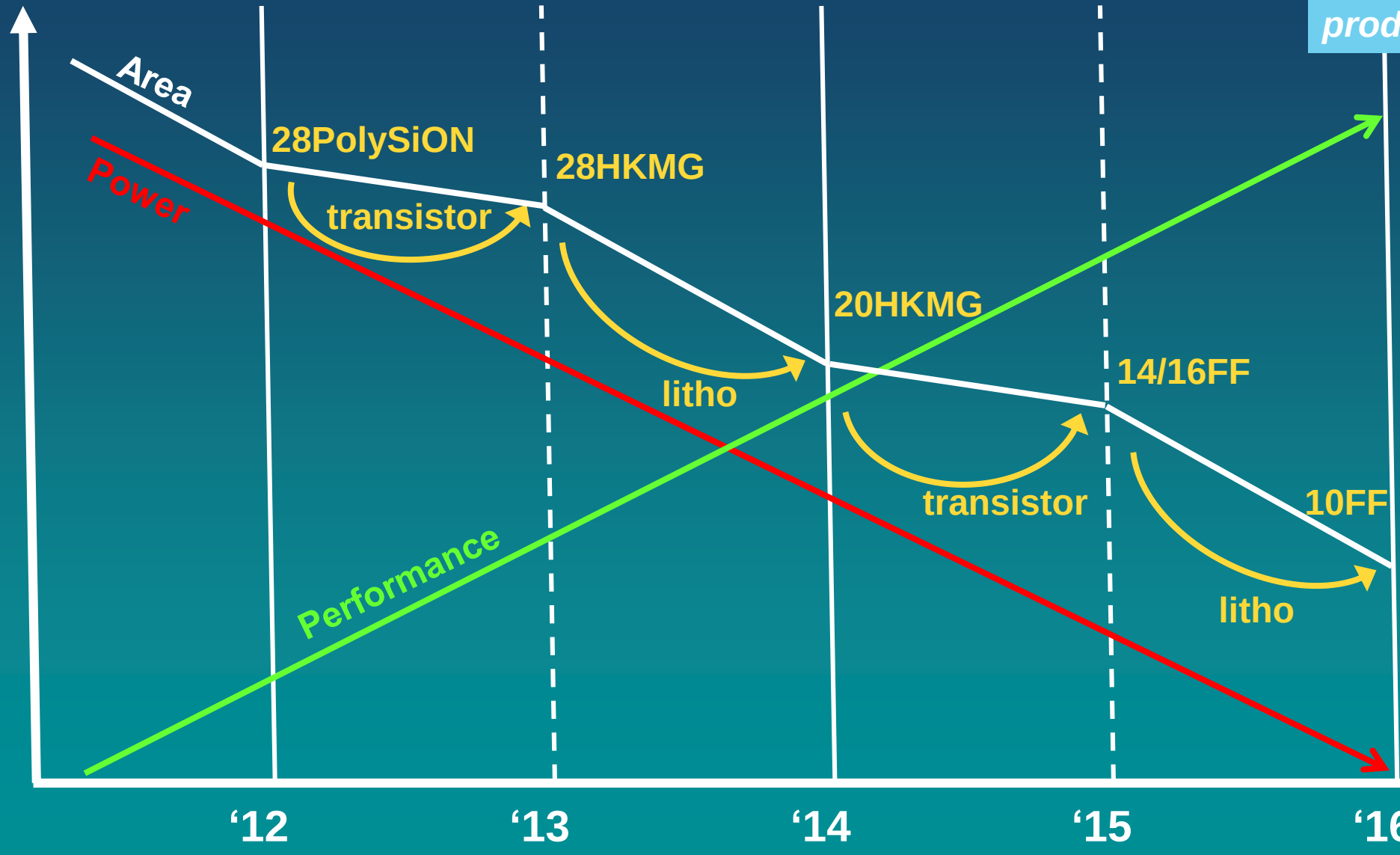
Moore's Law

...over the history of computing hardware, the number of transistors in a dense integrated circuit doubles approximately every two years

- Gordon Moore, Intel co-founder, 1965

Corollary: Economics dictate cost per transistor must also decrease!

Continuous innovation has provided **annual** technology cadence



Aligned with annual mobile product launch cadence

Full area scaling on regular 2-year cadence

Incremental area scaling on transistor upgrade nodes

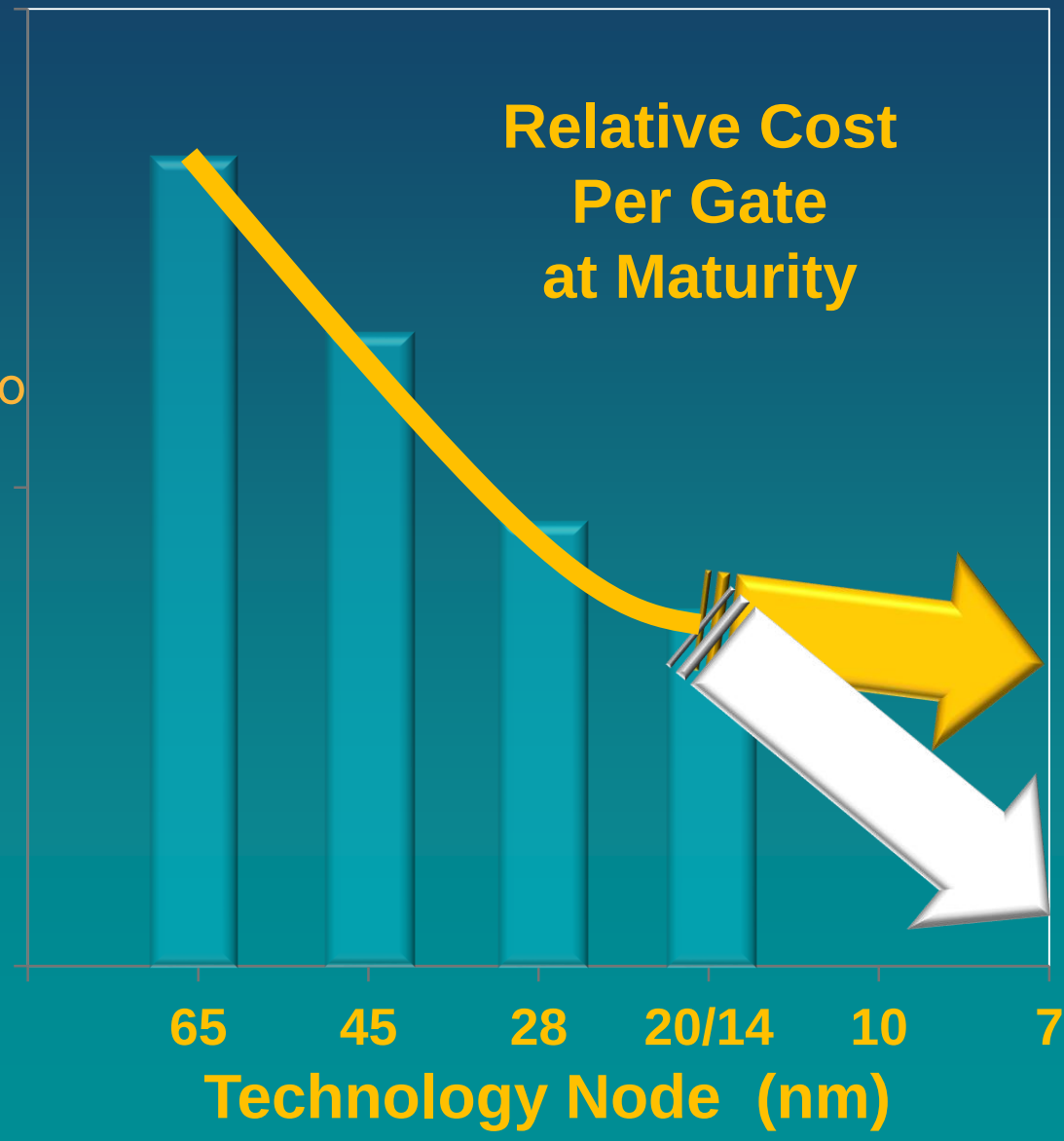
Annual Performance & Power improvements

Diminishing CMOS Cost Improvement – Patterning Cost

Process complexity increasing by mask count increase

Aggressive pitch scaling to improve die cost by area scaling

Threat for putting more functionality in the same area



???
"traditional path"
- Primary culprit: litho cost

-New Materials Opportunities
-multi-pattern cost down
-EUV lithography
-Design/tech co-optimization
- ….

193i Multi-patterning cost explosion

Need solutions to reduce litho cost and multi-patterning requirements

Patterning Cost

Can we find a cost-effective litho solution for N7?

EUV Lithography

Low Cost 193i Multi-patterning

Need cost effective EUV <u>AND</u> 193i litho solution !

EUV Potential Benefits in N7

Reduced wafer/die cost due to reduced mask count and better shrink

-reducing MEOL complexity by 2D Metal1 intra-cell routing

-replacing repetitive depo & litho steps in 193i

Potential yield gains

-reduced mask count

-reduced number of vias (DFM)

Potential area gains by less restrictions in layout

EUV/N7 Timing

When is decision point for N7?

AT MOST within one year from now (Q4'15)

Need to demonstrate readiness of EUV in all aspects (source, resist, mask, etc.) in order to irreversibly integrate into N7 flows

Demonstrate in a "reversible" manufacturing environment (14nm/10nm?) as an option

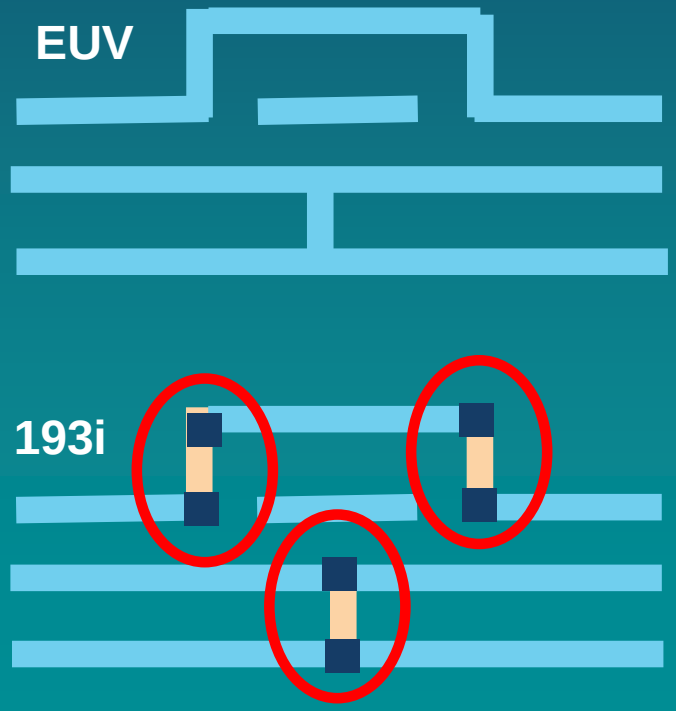
2D EUV layout benefits

Able to employ jogs

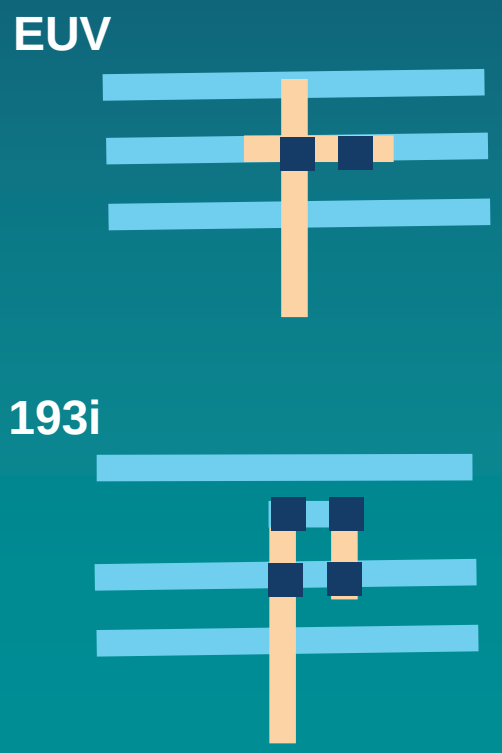
Reduced #vias (better yield)

Less min length (area) wires

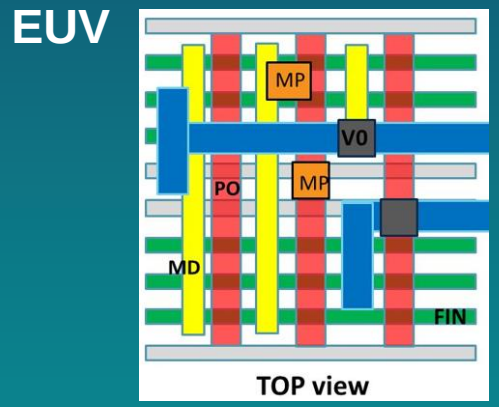
Able to connect to neighbor wire

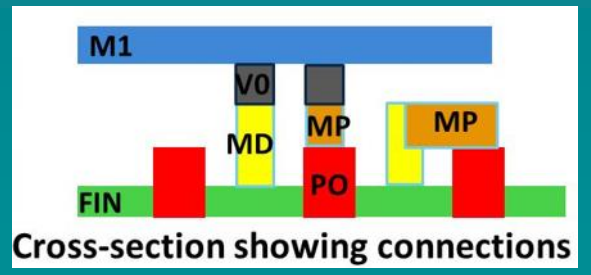


Better freedom for redundant via insertion

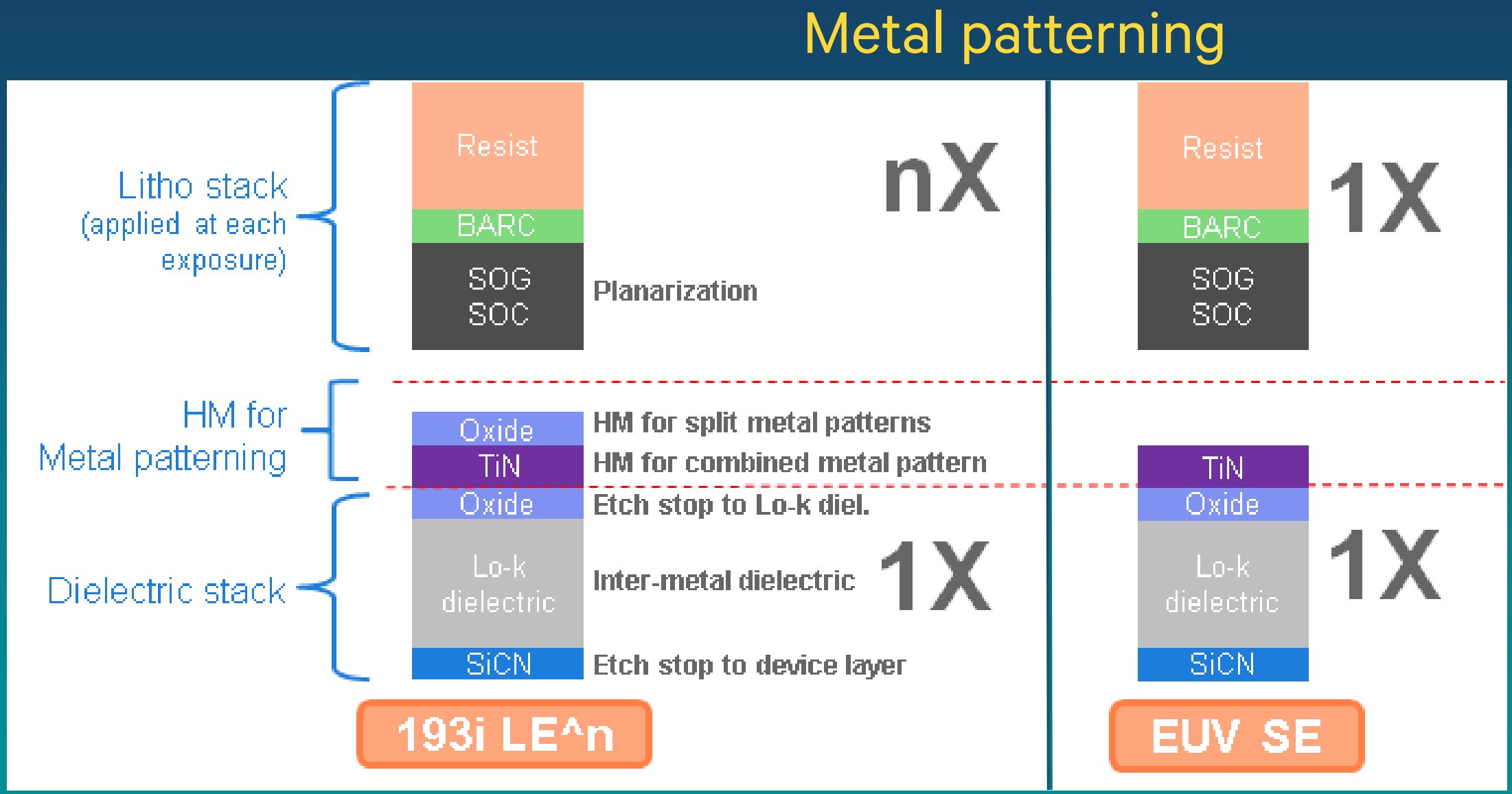


Reduced MOL complexity by 2D M1

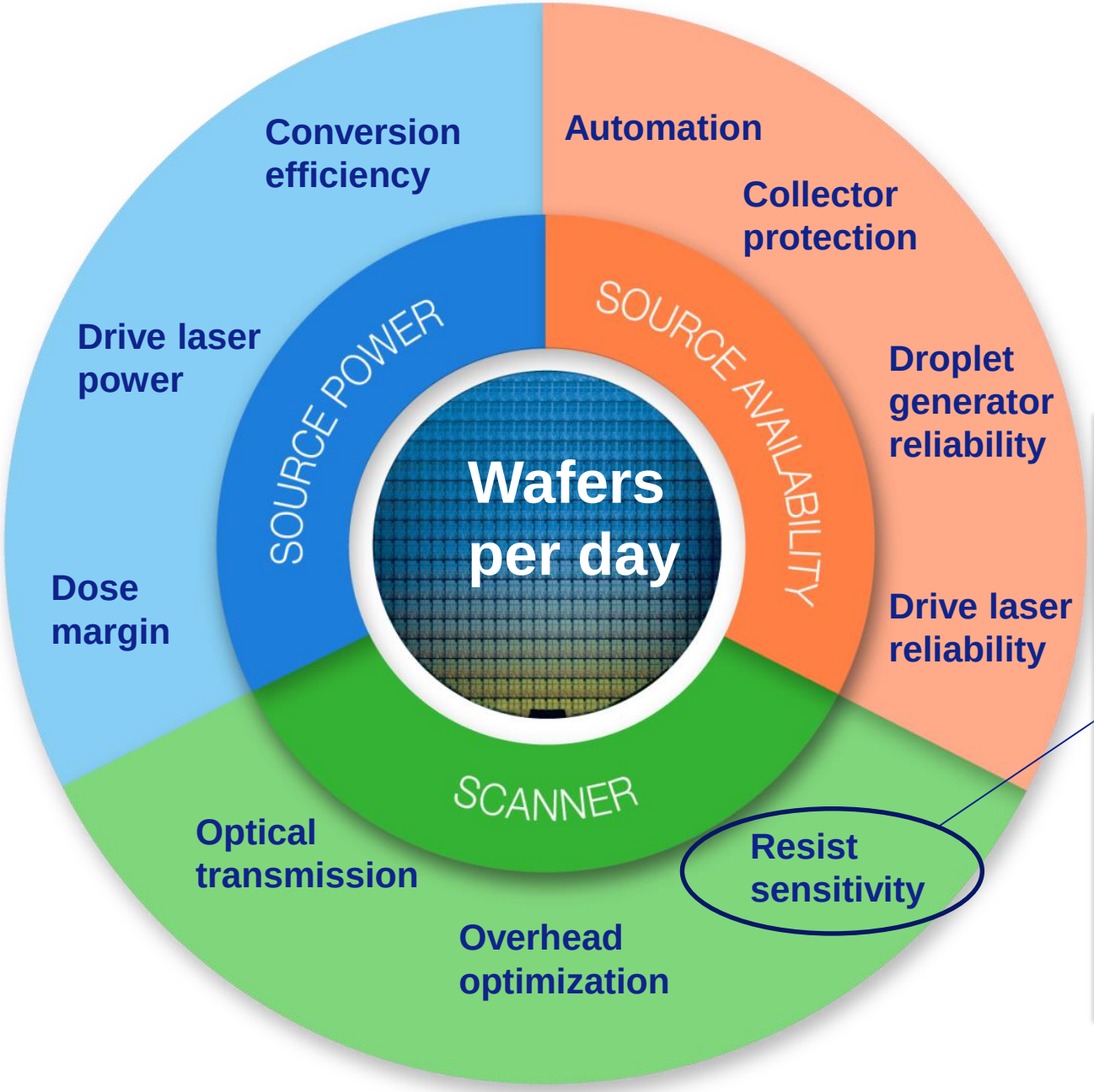


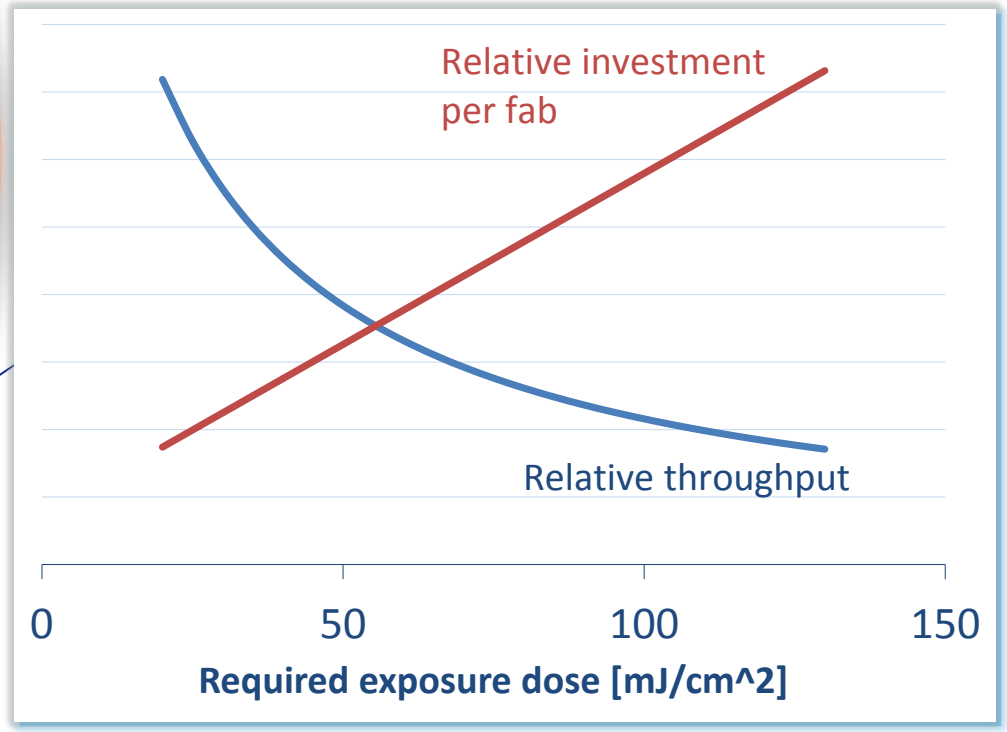


Number of deposition, litho, and etch steps reduced with EUV

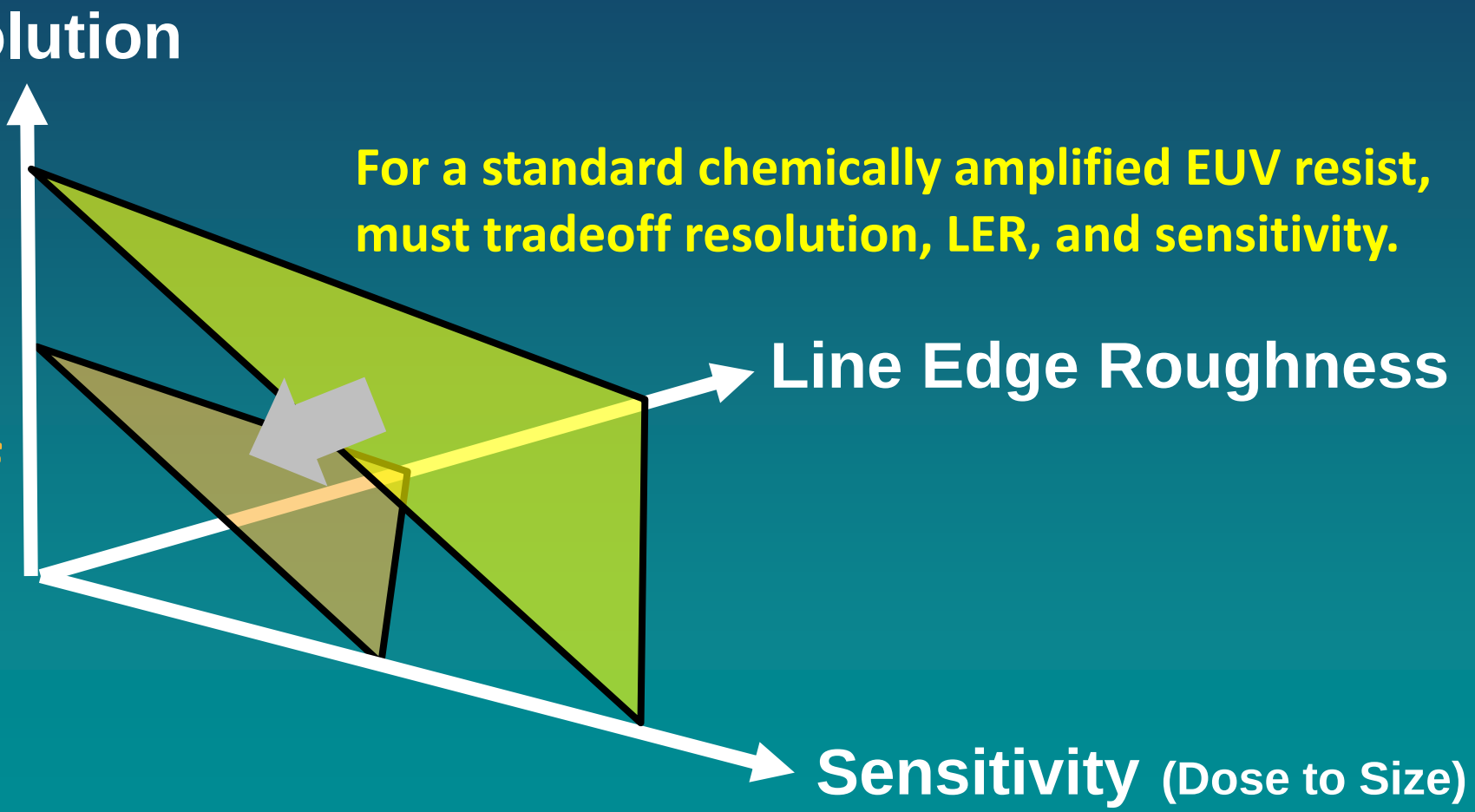


EUV productivity is determined by a number of factors





Need for highly-sensitive EUV resists for increased productivity while meeting resolution and LER requirements



For a standard chemically amplified EUV resist, must tradeoff resolution, LER, and sensitivity.

Break the RLS tradeoff

- new EUV resist materials including developers, cleans, top coats, etc

For all 3 factors, smaller is better

Summary

Mobile revolution will continue to rely on Moore's Law to deliver increased integration, power reduction and value to consumers

Patterning costs are exploding and may limit expected cost reduction in the future – innovation is needed

- 193i multi-patterning cost reduction, EUV, DSA, etc.

N10 will not use EUV lithography. EUV is a candidate for N7 to reduce patterning cost

- Full feasibility for practical manufacturability must to be demonstrated by Q4'15 for irreversible commitment to EUV in N7
- Need to demonstrate EUV as an optional step in existing manufacturing environment with 193i as backup (14nm/10nm?)

Thank you!